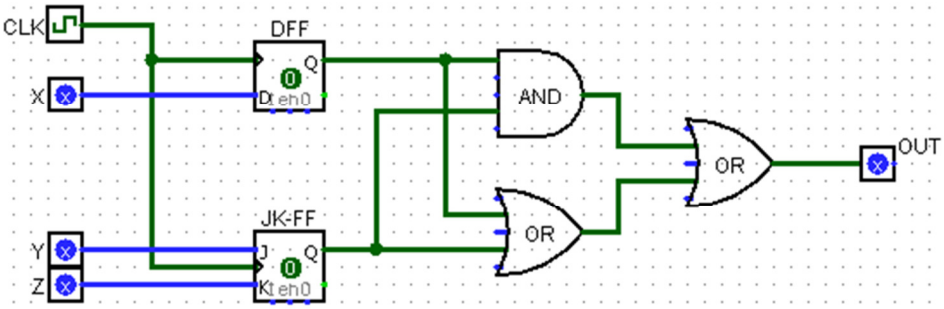
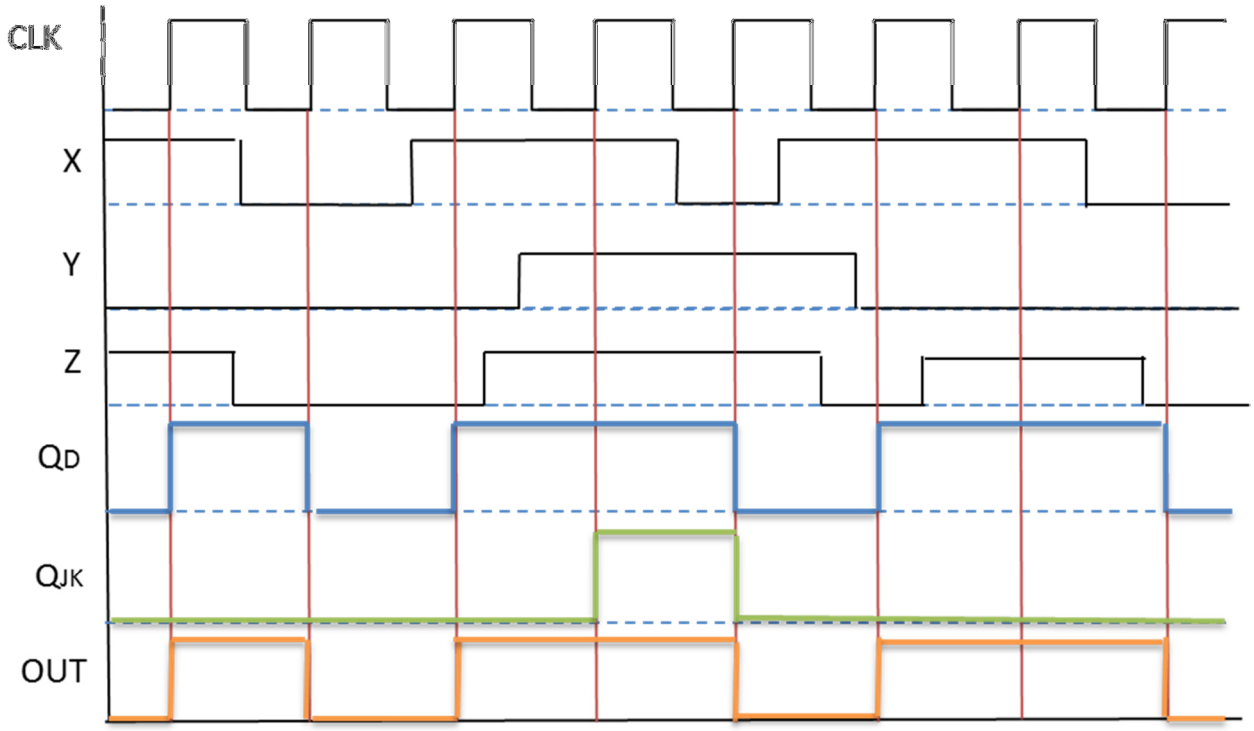
From the circuit below complete the timing diagram, assume positive edge and Qs=0 at t=0





J	K	Present State (Q)	Next State (Q)
0	0	0	No Change
0	0	1	
0	1	0	Reset
0	1	1	
1	0	0	Set
1	0	1	
1	1	0	Toggle
1	1	1	

D	Present State (Q)	Next State (Q)
0	0	0
0	1	
1	0	1
1	1	