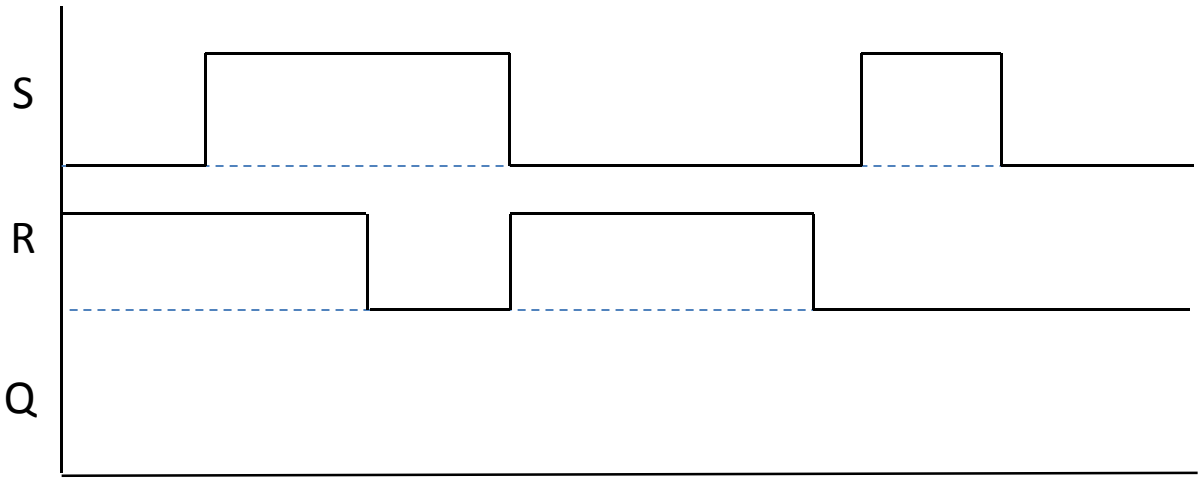
CSCI 255 – Intro to Embedded Systems
Homework #8
Fall 2013

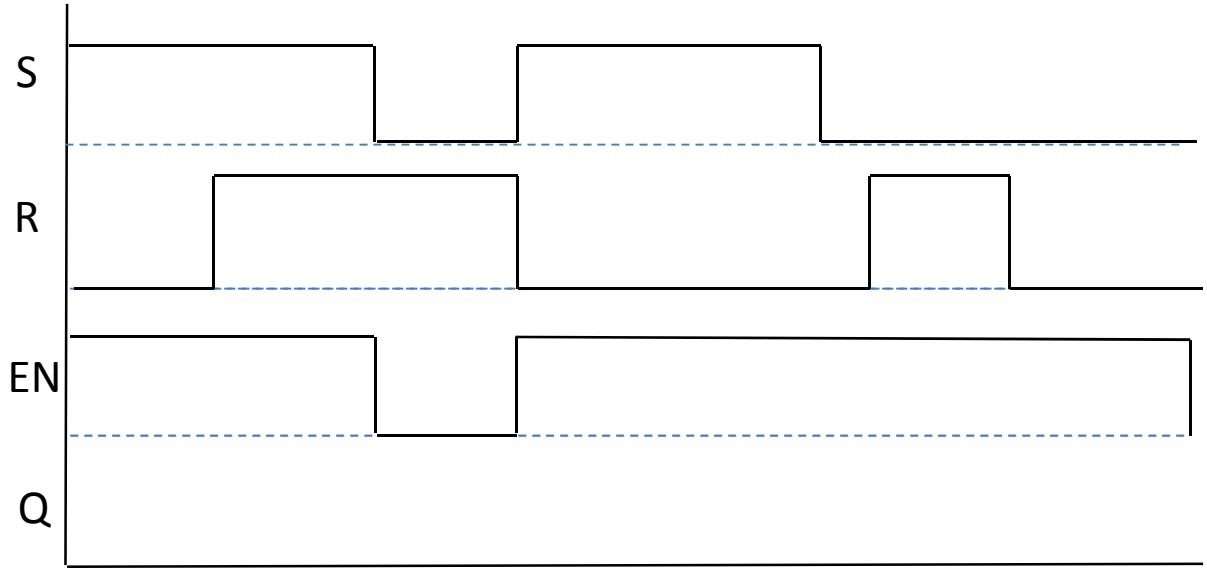
Work must be done individually

Due: **10/23/2013** by **beginning of class**

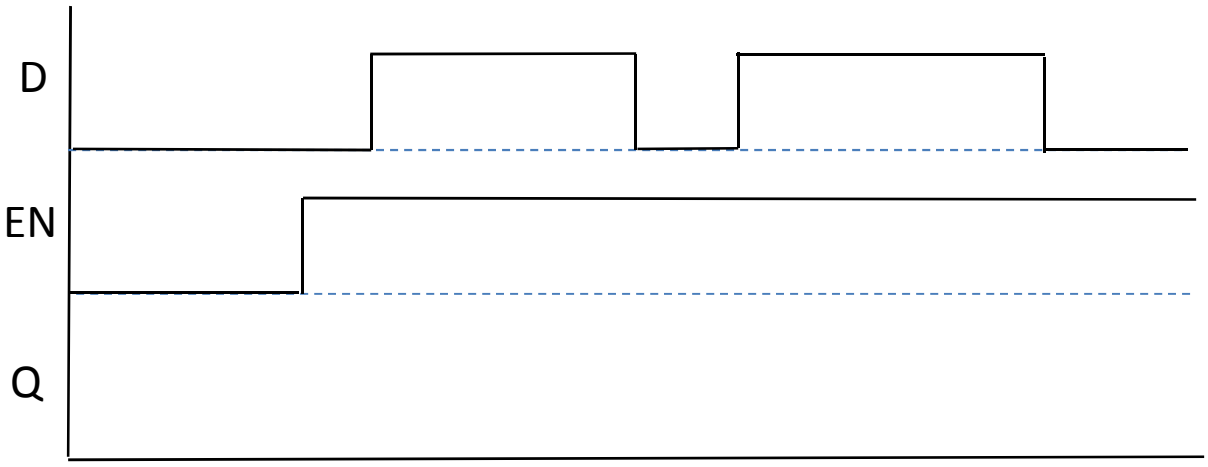
1. **Draw the Q-output signal when analyzing the SR-Latch inputs below: (Assume Q=0 @ t=0)**



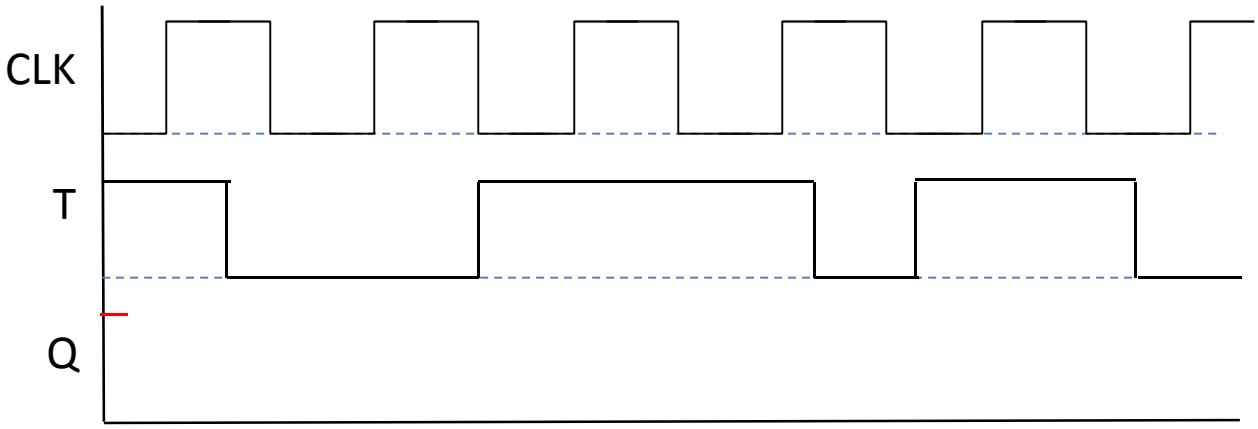
2. **Draw the Q-output signal when analyzing the SR-Latch inputs below: (Assume Q=1 @ t=0)**



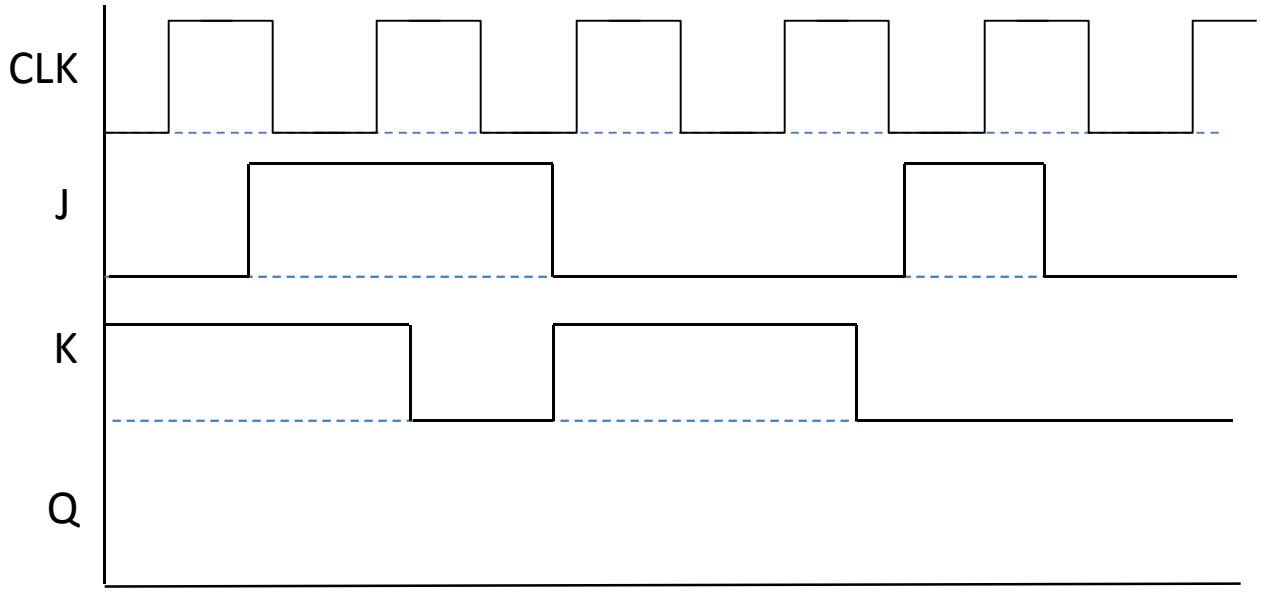
3. **Draw the Q-output signal when analyzing the D-Latch inputs below: (Assume Q=1 @ t=0)**



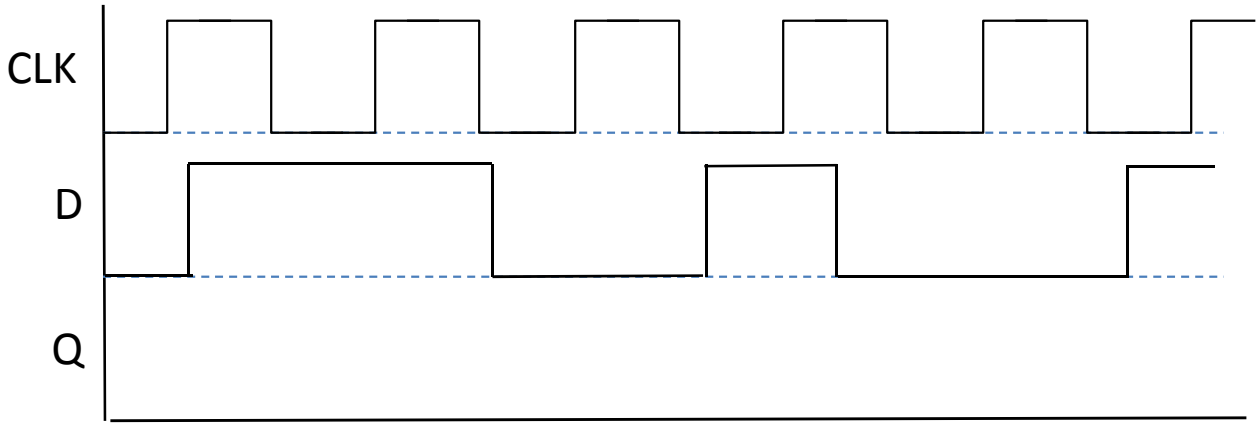
4. **Draw the Q-output signal when analyzing the T-FF inputs below: (Assume Positive Edge and Q value=1 @ t=0 is given)**



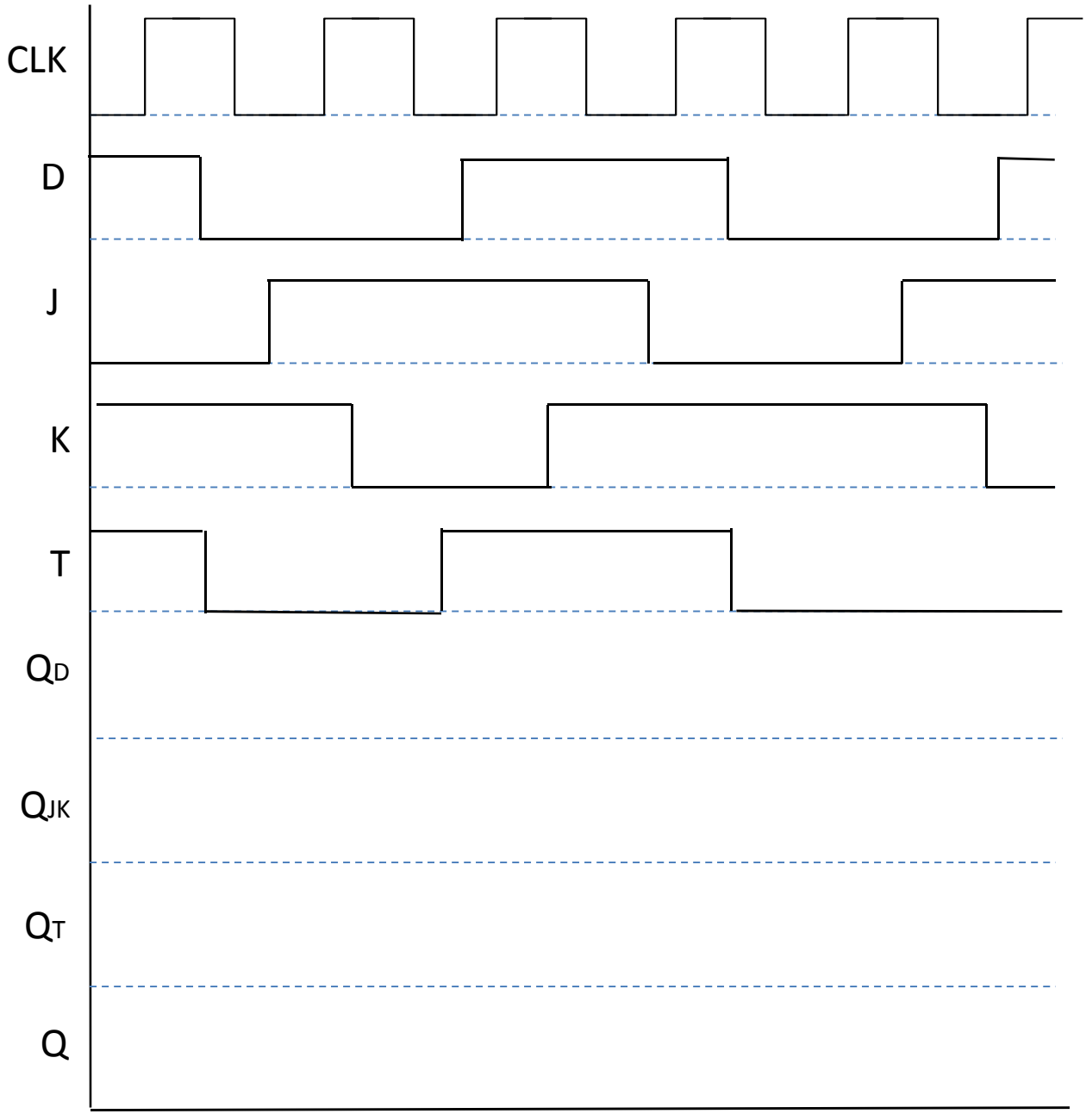
5. **Draw the Q-output signal when analyzing the JK-FF inputs below: (Assume Positive Edge and Q=0 @ t=0)**



6. **Draw the Q-output signal when analyzing the D-FF inputs below: (Assume Negative Edge and Q=0 @ t=0)**



7. **Draw the Q-output signals of each Flip-flop below to their corresponding signals, assume:**
   - **D-FF and T-FF react to the negative edge**
   - **JF-FF react to the positive edge**
   - **Q = (Q_D + Q_T) xor Q_{JK} (Remember that combinational circuitry does not react to CLK)**
   - **Assume Q_D ,Q_T ,Q_{JK} = 0 @ t=0**



8. **From the circuit below complete the timing diagram, assume positive edge and Qs=1 at t=0**