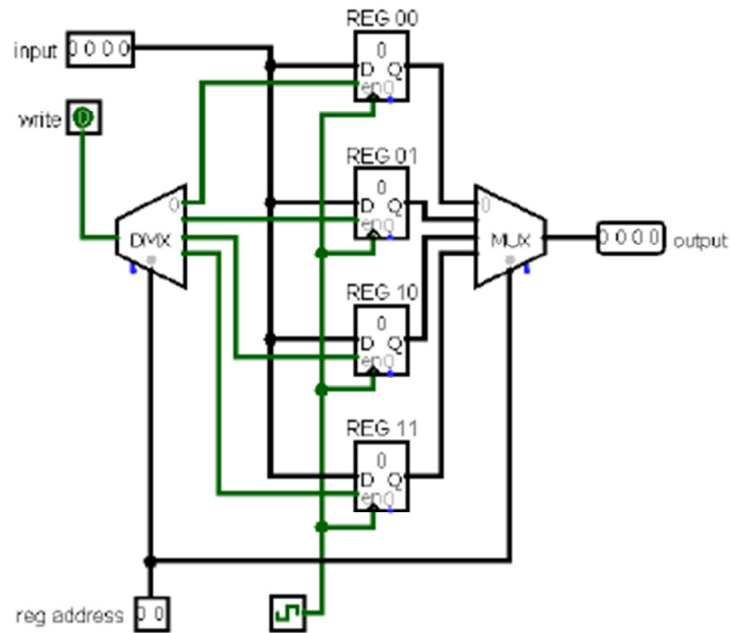


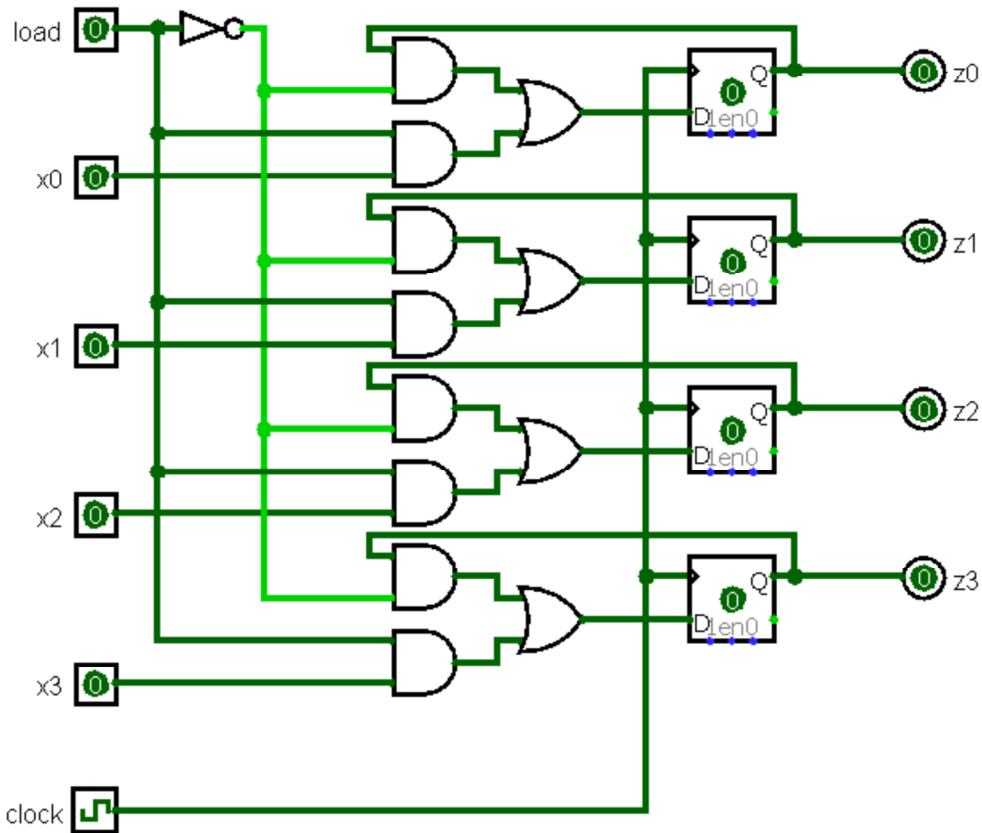
Due: **11/13/2013** at the beginning of class -- **Work must be done individually**

1. Fill-out the blanks of the table below corresponding to the register bank circuit below:



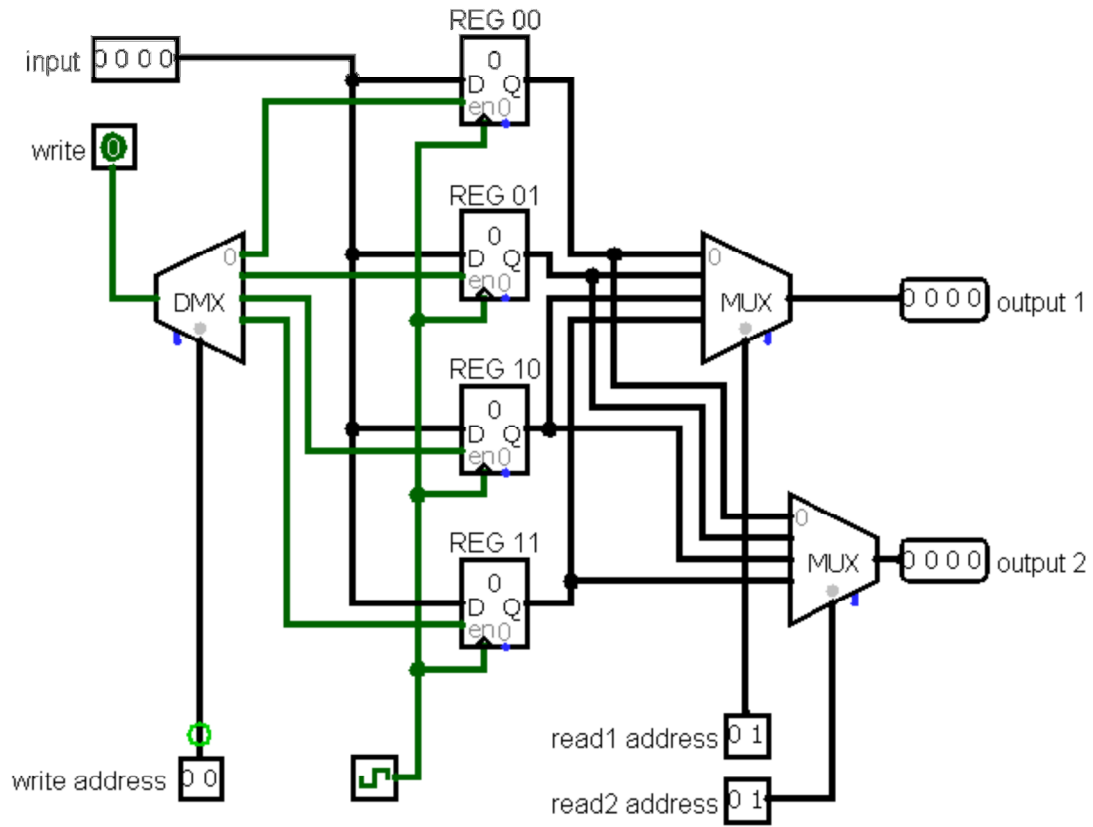
	Prior	Cycle 1	Cycle 2	Cycle 3
Reg 00	1110			
Reg 01	0100			
Reg 10	0101			
Reg 11	0011			
input	0000	1011	0101	1001
output	0000			
Write	0	1	1	1
Reg Addr	00	01	11	10

2. Fill-out the blanks of the table below corresponding to the register parallel load circuit below:



	Prior	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5
D-FF (Z0)	1					
D-FF (Z1)	1					
D-FF (Z2)	0					
D-FF (Z3)	0					
load	0	1	1	1	0	1
$X_3X_2X_1X_0$	1110	0110	1110	0001	1111	1010

3. Fill-out the blanks of the table below (next page) corresponding to the register bank circuit below:



	Prior	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5
Reg 00	1110					
Reg 01	0100					
Reg 10	0101					
Reg 11	0011					
input	0010	1111	0001	1011	0111	1000
Output1	0000					
Output2	0000					
Read 1 Address	00	10	00	11	00	01
Read 2 Address	10	11	01	00	00	10
Write	0	1	1	0	0	1
Write Address	00	00	11	11	01	01

	Prior	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5
Reg 00	1110					
Reg 01	0100					
Reg 10	0101					
Reg 11	0011					
Output1 Top Mux of Reg Bank	0100					
Output2 Bottom Mux of Reg Bank	0010					
Read 1 Address	00	00	10	11	11	00
Read 2 Address	10	01	01	10	01	10
ALU MUX OUTPUT	0000					
ALU Mux Select	00	10	00	11	00	01
Write	0	1	0	0	0	1
Write Address	00	10	10	01	11	00